Annexure – IX

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002

PROFORMA FOR SUBMISSION OF INFORMATION AT THE TIME OF SENDING THE FINAL REPORT OF THE WORK DONE ON THE PROJECT

1. TITLE OF THE PROJECT	**Study of Germanium / III-V Compound Semiconductors as Channel Materials for Nano Scale Devices**
2. NAME AND ADDRESS OF THE PRINCIPAL INVESTIGATOR	**Dr Rakesh Vaid, Professor, Dept of Electronics, University of Jammu, Jammu-180 004**
3. NAME AND ADDRESS OF THE INSTITUTION	**UNIVERSITY OF JAMMU, Baba Saheb Ambedkar Road, New Campus, Jammu – 180006 (INDIA)**
4. UGC APPROVAL LETTER NO. AND DATE	**File No- 43-296/2014(SR) Dated: 5 August 2015**
5. DATE OF IMPLEMENTATION	**01/07/2015**
6. TENURE OF THE PROJECT	**01/07/2015 to 30/06/2018 (3 years)**
7. TOTAL GRANT ALLOCATED	**Rs. 10, 49, 500/-**
8. TOTAL GRANT RECEIVED	**Rs. 10, 45, 000/-**
9. FINAL EXPENDITURE	**Rs. 10, 44, 943/-**
10. TITLE OF THE PROJECT	**Study of Germanium / III-V Compound Semiconductors as Channel Materials for Nano Scale Devices**
11. OBJECTIVES OF THE PROJECT	**(Please see the detailed Progress report attached)**
12. WHETHER OBJECTIVES WERE ACHIEVED	**Yes: (see the detailed Progress report attached)**
13. ACHIEVEMENTS FROM THE PROJECT	**Please see the detailed Progress report attached**
14. SUMMARY OF THE FINDINGS	**Please see the detailed Progress report attached**
15. CONTRIBUTION TO THE SOCIETY	**Please see the detailed Progress report attached**

16. WHETHER ANY PH.D. ENROLLED/PRODUCED OUT OF THE PROJECT **NO**

17. NO. OF PUBLICATIONS OUT OF THE PROJECT **Please see the detailed Progress report attached**

(PRINCIPAL INVESTIGATOR)

Dr. RAKESH VAID
Principal Investigator
UGC Major Research Project
University of Jammu
Jammu

(REGISTRAR)

Registrar
University of Jammu

(Seal)

05/09/18

UNIVERSITY GRANTS COMMISSION

MAJOR RESEARCH PROJECT

FINAL PROGRESS REPORT

STUDY OF GERMANIUM / III-V COMPOUND SEMICONDUCTORS AS CHANNEL MATERIALS FOR NANOSCALE DEVICES

UGC Reference No: 43-296/2014(SR) Dated: August 05, 2015
MRP-MAJOR-ELEC-2013-22797

SUBMITTED TO

University Grants Commission
Bahadur Shah Zafar Marg, New Delhi
NEW DELHI – 110 002

By
Dr. Rakesh Vaid
Department of Electronics
University of Jammu
Jammu – 180 006, J&K, INDIA

Detailed Research Work

1. Project Title:

STUDY OF GERMANIUM / III-V COMPOUND SEMICONDUCTORS AS CHANNEL MATERIALS FOR NANOSCALE DEVICES

2. Objectives of the Project:

The proposed objectives of this project were as under:

- **By Simulation Approach**

a) To simulate single and double gate nano-MOSFETs with III-V compounds as channel materials such as Ge/GaAs/ InP/ InAs/ InSb etc.

b) To optimize various device parameters such as Inversion mobile charge, Qc/insulator capacitance, average velocity, quantum capacitance, transconductance to current ratio (g_m/Id), voltage gain as well as carrier injection velocity using simulations for experimental studies.

c) To model the MOS cap devices for future MOSFETs devices with new channel materials like Ge, GaAs, InAs, InSb etc and Al_2O_3, ZnO, HfO_2 as High-K oxide materials for improving the device performance and for memory device application.

d) To investigate the various effects of oxide thicknesses (T_{OX}), high dielectric constants, temperature etc. on the performance of nano-MOSFETs by simulation approach.

e) To develop and analyze analytical models for these nanoscale devices.

By Experimentation Approach

The following MOSCAP studies has been undertaken in collaboration with CEN at IIT Mumbai:

- $Si/HfO_2/Al$ MOScap
- $Si/HfO_2/Pt$ MOScap
- $Ge/SiO_2/Al$ MOScap
- $Ge/HfO_2/Al$ MOScap

- Ge/HfO_2/Al MOScap
- Ge/Al_2O_3/Al MOScap

The following studies were undertaken:

- Conductivity (C-V, I-V, J-V characteristics)
- Equivalent oxide thickness (EOT)
- Charges in the oxide
- Leakage current
- Oxide breakdown strength,
- Interface sate density (D_{it}) etc.

3. Achievements from the Project:

The proposed structures have been designed and analyzed using simulation approach and results have been verified by the detailed data generated using various simulators either analytically or experimental data reported in the literature.

The experimental exploration of the proposed structures and devices has been carried out using the fabrication facilities available at IIT Mumbai under INUP program of the DST. In this regard, the following medium term projects were undertaken:

a. Fabrication and Characterization of MOS capacitor Using Ge/GaAs/InAs substrate to be used for future nanoscale MOSFETs. **(completed)**

b. Fabrication & Characterization of Pt/HfO2/SiON/Ge/Si-MOS capacitor for non-volatile memories. **(completed)**

c. To fabricate and study the electrical characteristics of Pt/TiO2/Au/SiON/Si structure employing metal nano-dots for non-volatile memory applications. **(completed)**

d. Fabrication and characterization of silicon based hybrid solar cell employing high k dielectrics. **(completed)**

Simulation and modeling software Silvaco ATHENA/ATLAS which has been acquired under this project was used to generate the data for validation with the experimental results as well as analytical formulations. Besides, the fabrication of a simple MOS device using high mobility III-V compound semiconductors replacing silicon in the channel as well as in the source and drain regions has been explored and the various

results obtained has been published in various international journals and conference proceedings.

4. Summary of the findings

a. Extensive simulations of the proposed structures have been performed to generate data. The simulation results so obtained were used to understand the devices physics.

b. Various MOS capacitors were fabricated under INUP programme in collaboration with CEN at IIT Mumbai.

c. The device physics and results for different physical parameters of the device were determined and analyzed.

d. The results so obtained have been published in various international journals and conferences of repute (refer the list of publications).

5. Contribution to the Society

After more than 20 years of basic nanoscience research, the applications of nanotechnology are delivering in both expected and unexpected ways on nanotechnology's promise to benefit society. Transistors, the basic switches that enable all modern computing have gotten smaller and smaller through nanotechnology. Smaller, faster, and better transistors may mean that soon your computer's entire memory may be stored on a single tiny chip. Keeping in view all these prerequisites, we mainly focused on the scaling of nanoscale devices using III-V compound semiconductor materials and achieved good results. Furthermore, we fabricated various MOS capacitors using high-k dielectric materials and achieved the capacitance density, EOT and leakage current density as demanded by ITRS roadmap. The improvement in such parameters will definitely be beneficial to the society in numerous ways and will help the researchers working in this area for more improved designs.

6. Details of the Publications resulting from the Project work

Research Papers published in Referred Journals/conference proceedings

1. Renu Rajput, Richa Gupta, Rakesh K Gupta, Ajit Khosla, **Rakesh Vaid**, "Fabrication and characterization of n-Si/SiON/metal gate structure for future MOS technology" Microsystems Technologies, 24 (10), 4179-4185, Springer Berlin Heidelberg, 2018 **[ISSN No: 0946-7076] Impact factor: 1.581**.

2. Richa Gupta and **Rakesh Vaid,** "Structural and Electrical Characteristics of Oxygen Annealed ALD-ZrO2/SiON Gate Stack for Advanced CMOS Devices" ***ECS Transactions***, vol. 85, no. 13, pp. 1481-1487, 2018. **doi: 10.1149/08513.1481ecst**

3. **Rakesh Vaid,** Dulen Saikia, Richa Gupta, "Argon Annealed ALD-ZrO2/SiON Gate Stack for advanced CMOS devices", ***ECS Transactions***, vol. 77, no. 5, pp. 51-55, 2017. **doi: 10.1149/07705.0051ecst**

4. Dulen Saikia, Pallabi Phukan and **Rakesh Vaid**, "Optimizing the Physical Properties of CBD PbSe Thin Films for Photovoltaic Application", ***ECS Transactions***, vol. 77, no 6, pp. 95-106, 2017. **doi: 10.1149/07706.0095ecst**

5. Richa Gupta, Renu Rajput, Rakesh Prasher and **Rakesh Vaid,** "Structural and electrical characteristics of ALD-HfO_2/n-Si gate stack with SiON interfacial layer for advanced CMOS technology" ***Solid State Sciences***, vol. 59, pp. 7-14, September 2016 [ISSN No: 1293-2558] doi:10.1016/j.solidstatesciences.2016.07.001 **(Elsevier) Impact factor: 2.041.**

6. Richa Gupta and **Rakesh Vaid**, "TCAD performance analysis of high-K dielectrics for gate all around InAs nanowire transistor considering scaling of gate dielectric thickness", ***Microelectronic Engineering***, vol. 160, pp. 22-26, July 2016 [ISSN No: 0167-9317] doi:10.1016/j.mee.2016.02.057 **(Elsevier) Impact factor: 1.257.**

7. Richa Gupta and **Rakesh Vaid,** "Effect of Post Deposition Annealing on ALD-ZrO_2/SiON Gate Stacks for Advanced CMOS Technology" ***ECS Transactions***, vol. 74, no. 17, pp. 67-73, September 2016. **doi:10.1149/07517.0067ecst**

8. Renu Rajput and **Rakesh Vaid**, "Effect of Thermal and Forming Gas Annealing on the Characteristics of Si/SiON/Ti-Pt MOS Capacitor" ***Proc IEEE INDICON*** 2017 held at IIT Roorkee w.e.f. Dec 15-17, 2017.

9. Rakesh Prasher, Devi Dass & **Rakesh Vaid,** -Al/HfO_2/Si gate stack with improved physical and electrical parameters‖ ***Proc. IEEE 29th Int. conference on VLSI design*** held at Kolkatta, India w.e.f. Jan 4-8, 2016, pp. 334-337.

Paper Presented in Referred International/National Conferences

1. Richa Gupta and **Rakesh Vaid**, — I High-k based Gate Stacks for Advanced CMOS Devices" presented in the International Conference on Nanoscience and Nanotechnology (ICNN-2017) held at Babasaheb Bhimrao Ambedkar University, Lucknow, Uttar Pradesh, India, w. e. f. September 22-24, 2017. **(Invited)**

2. Richa Gupta and **Rakesh Vaid**, "Effect of Post Deposition Annealing on the Structural and Electrical Characteristics of ALD-ZrO2/SiON Gate Stack" accepted for presentation in the Second National Conference on Recent Developments in Electronics (NCRDE) to be held at University of Delhi South Campus, New Delhi w.e.f. Feb. 17-18, 2017. **(Invited)**

3. Richa Gupta and **Rakesh Vaid**, "Emerging high-k materials for Nano CMOS device applications", presented in India International Science Festival (IISF) - Young Scientists' Conclave (YSC), 2016.

4. Richa Gupta and **Rakesh Vaid,** "Fabrication and Characterization of high-k based nano-MOS capacitors for advanced CMOS applications" presented in "National seminar cum workshop on advances in science and technology and pertinent need of instrumentation" held at Department of Physics and IQAC Sibsagar College, Joysagar, 2016. **(Invited)**

Paper Presented Abroad

1. Paper Presentation in the 231st ECS meeting at **New Orleans (USA)**, May 28 to June 01 2017.
2. Invited Talk in the IEEE UK and Ireland section on June 05, 2017 in the **University of Manchester, UK.**
3. Paper Presentation in the 233rd ECS meeting at **Seattle (USA)**, May 13-17, 2018.

Dr. RAKESH VAID
Principal Investigator
UGC Major Research Project
University of Jammu
Jammu

Annexure - III

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002

STATEMENT OF EXPENDITURE IN RESPECT OF MAJOR RESEARCH PROJECT

1. Name of Principal Investigator: **Dr Rakesh Vaid**

2. Dept. of Principal Investigator: Dept of Electronics

3. University/College: University of Jammu, Jammu

4. UGC approval Letter No. and Date: File No- 43-296/2014(SR) Dated: 5 August 2015

5. Title of the Research Project: **Study of Germanium / III-V Compound Semiconductors as Channel Materials for Nano Scale Devices**

6. Effective date of starting the project: Sanctioned: 01/07/2015

7. a. Period of Expenditure: **01/07/2015 to 30/06/2018**

b. Details of Expenditure

Name of the Item	Amount Approved (Rs.)	Expenditure incurred (Rs.)
Books &Journals	Nil	Nil
Equipment	**10,00,000/-**	**9,99,989/-**
Contingency	**40,500/-**	**40, 454/-**
Field Work/Travel	Nil	Nil
Hiring Services	Nil	Nil
Chemicals/Glassware	Nil	Nil
Overhead	**4500/-**	**4500/-**
Total	**10, 45, 000/-**	**10, 44, 943/-**

c. Staff -N. A-

Date of appointment: (i) -N. A-

S.No	Items	From	To	Amount Approved (Rs.)	Expenditure incurred (Rs.)
1.	Honorarium to the PI (Retired teachers) @ Rs. 18000/-	-N. A-			
2.	Project Fellow	-N. A-			

1. It is certified that the appointment have been made in accordance with the terms and conditions laid down by the commission.
2. If as a result of check or audit objection some irregularity is noticed at later date, action will be taken to refund, adjust or regularize the objected amounts
3. Payment @ revised rates shall be made with arrears on the availability of additional funds.
4. It is certified that **Rs. 10, 44, 943/- (Rs. Ten lakh forty four thousand nine hundred forty three only)** out of the total grant of **Rs. 10, 45, 000/- (Rs. Ten lakh forty five thousand only) released** for the years **01/07/2015 to 30/06/2018** under the scheme for Major Research Project entitled "**Study of Germanium / III-V Compound Semiconductors as Channel Materials for Nano Scale Devices**" vide UGC letter No. 43-296/2014(SR) dated: August, 05, 2015 has been utilized for the purpose for which it was sanctioned with the terms and conditions laid down by University Grant.

   An unspent balance of **Rs. 57/- (Rs. Fifty seven only)** has been refunded to the Secretary UGC vide instrument no JAKA140818919020 dated: 14/08/2018 into the Account no: 8627101002122 of Canara Bank of the UGC Branch, New Delhi.

Signature of the Principal Investigator

Dr. RAKESH VAID
Principal Investigator
UGC Major Research Project
University of Jammu
Jammu

Registrar

Registrar
University of Jammu
05/08/18

Statutory Auditor (Govt. Internal Auditor/ Chartered Accountant)

C. Gupta & Co. Chartered Accountants FRN - 001198 N Jammu

Annexure - V

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002

Utilization Certificate

It is certified that the grant of **Rs. 10, 44, 943/- (Rs. Ten lakh forty four thousand nine hundred forty three only)** out of the total grant of **Rs. 10, 45, 000/- (Rs. Ten lakh forty five thousand only) released** for the years **01/07/2015 to 30/06/2018** for Major Research Project entitled "**Study of Germanium / III-V Compound Semiconductors as Channel Materials for Nano Scale Devices**" vide UGC letter No. 43-296/2014(SR) dated: August, 05, 2015 has been utilized for the purpose for which it was sanctioned with the terms and conditions laid down by University Grant.

An unspent balance of **Rs. 57/- (Rs. Fifty seven only)** has been refunded to the Secretary UGC vide instrument no JAKA140818919020 dated: 14/08/2018 into the Account no: 8627101002122 of Canara Bank of the UGC Branch, New Delhi.

If as a result of check or audit objection some irregularity is noticed at later date, action will be taken to refund, adjust or regularize the objected amounts.

Signature of the Principal Investigator
Dr. RAKESH VAID
Principal Investigator
UGC Major Research Project
University of Jammu
Jammu

Registrar
Registrar
(Seal)

Statutory Auditor
(Govt. Internal Auditor/ Chartered Accountant)
(Seal)

Annexure XI

Final Report Assessment / Evaluation Certificate

(Two Members Expert Committee Not Belonging to the Institute of Principal Investigator)

(to be submitted with the final report)

It is certified that the final report of Major Research Project entitled "**Study of Germanium / III-V Compound Semiconductors as Channel Materials for Nano Scale Devices** by **Prof. Rakesh Vaid** of **Department of Electronics, University of Jammu** has been assessed by the committee consisting the following members for final submission of the report to the UGC, New Delhi under the scheme of Major Research Project.

Comments/Suggestions of the Expert Committee:-

→ Good work done

→ Excellent Publications

Name & Signatures of Experts with Date:-

	Name of Expert	University/College name	Signature with Date
1.	Prof. B. C. Yadav	Dept. of Physics, School for Physical & Decision Sciences, BBAU, Lucknow, U.P. India	25/7/18
2.	Dr. M. Tariq Banday	Dept. of Electronics and Inst. Tech, University of Kashmir, Srinagar, J&K.	25/7/18

It is certified that the final report has been uploaded on UGC-MRP portal on Sept. 11, 2018.

It is also certified that final report, Executive summary of the report, Research documents, monograph academic papers provided under Major Research Project have been posted on the website of the University/College.

Registrar
(Registrar)
University of Jammu
05/09/18